# METHOD FOR POLISHING SEMICONDUCTOR WAFER AND POLISHING PAD FOR THE SAME

## BACKGROUND OF THE INVENTION

The present invention relates to methods for polishing a semiconductor wafer and to polishing pads for the same. In particular, the present invention relates to polishing pads including a plurality of grooves for use in chemical mechanical polishing equipment designed for semiconductor wafers, and to methods for polishing a semiconductor wafer using such polishing pads.

Semiconductor devices have been miniaturized significantly in recent years. In order to accomplish the miniaturization, a variety of new technologies for fabricating a semiconductor device have been developed. Among the technologies, multilevel interlayer technology in which an interconnect layer of metal materials and an interconnect layer of insulating materials are repeatedly mutilayered contributes greatly to further miniaturization and high functionality of the semiconductor devices, but this technology also faces a number of technical challenges.

One of the challenges is to ensure the flatness of each interconnect layer. For example, the interconnect layers whose surfaces are not made flat but left uneven cause defocusing in a lithography process that is the key to the miniaturization of the semiconductor devices, which makes it impossible to form an interconnection pattern. To solve this challenge, chemical mechanical polishing (CMP) in which the surface of a semiconductor wafer is polished chemically and mechanically for planarization has often been used in recent years (see, e.g., Japanese Unexamined Patent Publication No. 11-58219).

Hereinafter, so-called belt-polishing CMP equipment, not conventional turntable-type CMP equipment, will be described with reference to the accompanying drawings.

FIG. 8A schematically shows a structure of a polishing section of the conventional

belt-polishing CMP equipment.

As shown in FIG. **8A**, a plurality of sheet-shaped polishing pads **101** of which the base material is composed of polyurethane foam are stuck on a belt-type surface plate **102**. With slurry **104** supplied from a nozzle **103** onto the polishing pads **101**, the surface plate **102** is driven. With a carrier **105** rotated, the surface of a semiconductor wafer **106** adhering by suction to the carrier **105** is pressed against the surface of the polishing pad **101**, thereby polishing the semiconductor wafer **106**. In order to activate (fuzz) the surfaces of the polishing pads **101**, a dresser **108** equipped on the bottom of a cylinder **107** is moved, whenever necessary, in the direction perpendicular to the drive direction of the surface plate **102** with the dresser **108** pressed against the polishing pad **101**.

FIG. **8B** shows one of the polishing pads **101** before it is stuck on the surface plate **102**. As shown in FIG. **8B**, a plurality of linear grooves **101a** spaced in parallel with one other are formed in the surface (polishing surface) of the polishing pad **101**. These grooves **101a** serve to efficiently supply the slurry **104** onto the surface (work surface) of the semiconductor wafer **106** in polishing the semiconductor wafer **106** and they are formed linearly and in parallel with the drive direction of the surface plate **102**.

In sticking the polishing pads **101** on the surface of the surface plate **102**, the polishing pads **101** adjacently arranged in the drive direction of the surface plate **102** are stuck slightly apart one from another.

The inventors recognize the following two problems of the conventional belt-polishing CMP equipment.

The first problem arises in the case where, as shown in FIG. **9A**, the multiple polishing pads **101** each having the multiple grooves **101a** are stuck on the surface of the belt-type surface plate **102** in such a manner that the grooves **101a** of each polishing pad **101** are spaced to align with the respective grooves **101a** of the adjacent polishing pad **101**.

When the semiconductor wafer **106** is polished by the CMP equipment as shown in FIG. **8A**, the surface plate **102** with the polishing pads **101** stuck thereon is driven at a

predetermined speed in the direction that goes away from the nozzle **103**. That is to say, the individual grooves **101a** of each polishing pad **101** move with fixed positions thereof kept relative to the semiconductor wafer **106**.

On the other hand, the carrier **105** with the semiconductor wafer **106** adhering thereto rotates at a given position. Therefore, as shown in FIG. **9B**, if the center portion of the semiconductor wafer **106** is matched in position to the groove **101a** provided in the center portion of the polishing pad **101**, a portion of the work surface of the semiconductor wafer **106** out of contact with the polishing surfaces of the polishing pads **101** occurs at the center portion thereof.

The polishing speed of the semiconductor wafer **106** by the polishing pads **101** degreases with increasing proximity to the center of the work surface of the semiconductor wafer **106**. As can be seen from the graph in FIG. **10A** illustrating the relation between the position within the wafer and the wafer surface thickness, the difference of the polishing speed within the wafer causes ununiformity in the wafer surface thickness such that the center portion of the work surface of the semiconductor wafer **106** has a greater thickness than the peripheral portion thereof. This ununiformity results from the fact that the individual grooves **101a** of one polishing pad **101** are in line with the respective grooves **101a** of the other consecutively-arranged polishing pads **101**. To be more specific, as shown in FIG. **10B**, concentric portions of the polished surface of the semiconductor wafer **106** each having a greater thickness than the surroundings occur with increasing proximity to the center of the polished surface of the semiconductor wafer **106**, so that a desired surface flatness cannot be obtained in the polished surface of the semiconductor wafer **106**. As has been described earlier, the thickness ununiformity causes defocusing in the lithography process that is the key to the miniaturization of semiconductor devices, which makes it impossible to form an interconnection pattern.

Next description will be made of the second problem of the conventional belt-polishing CMP equipment.

The second problem arises from the fact shown in FIG. **8B** that the grooves **101a** provided in the polishing surface of each polishing pad **101** are not formed in the both edge portions thereof. Because of such a structure, as shown in the sectional view in FIG. **11A**, the inside portion **A** of the polishing surface of the polishing pad **101** has a smaller contact area with a dresser **108** than the edge portion **B** thereof, so that the inside portion **A** of the polishing pad **101** has a greater pressure per unit area placed by the dresser **108** than the edge portion **B** thereof. The pressure difference causes the phenomenon in which the inside portion **A** of the polishing surface of the polishing pad **101** is removed by the dresser **108** more deeply than the edge portion **B** thereof. Thus, the inside portion **A** of the polishing pad **101** is thinner than the edge portion **B** thereof. As a result, as shown in FIG. **12A**, the inside portion **A** of the polishing pad **101** becomes thinned as compared to the edge portions **B** thereof every time the polishing pad **101** is activated by the dresser **108**, and finally the polishing pad **101** has a concave cross-sectional shape taken transversely of the drive direction of the pad. As can be seen from the graph in FIG. **12B** illustrating the relation between the position within the wafer and the wafer surface thickness, the polishing pad **101** having this concave cross-sectional shape polishes the semiconductor wafer **106** in such a shape that the peripheral portion of the semiconductor wafer **106** is polished more deeply than the center portion thereof. As a result, the semiconductor wafer **106** cannot obtain a desired surface flatness.

## SUMMARY OF THE INVENTION

To solve the conventional problems described above, an object of the present invention is to obtain a desired surface flatness of a semiconductor wafer using belt-polishing type polishing equipment.

To attain the foregoing object, a method for polishing a semiconductor wafer of the present invention is designed so that in sticking a plurality of polishing pads on a surface plate, grooves of the polishing pad are spaced not to align with respective grooves of the

adjacent polishing pad. Further, a polishing pad for a semiconductor wafer of the present invention has a structure in which multiple grooves of the polishing pad for a semiconductor wafer are provided over the entire width from edge to edge thereof in the direction perpendicular to the drive direction of the polishing pad.

To be more specific, in a method for polishing a semiconductor wafer according to the present invention, the semiconductor wafer is polished by continuously driving a surface plate on which a plurality of polishing pads are stuck, and the surface of each of the polishing pads is provided with a plurality of grooves each extending in the drive direction of the pad. The method comprises the steps of: sticking the plurality of polishing pads on the surface of the surface plate; and polishing the semiconductor wafer by pressing the wafer against the surface of each said polishing pad with the surface plate driven. In the sticking step, the polishing pads are stuck in such a manner that the grooves of each said polishing pad are spaced not to align with the respective grooves of the polishing pad adjacently arranged in the drive direction of the surface plate.

With the inventive method, in the step of sticking the polishing pads on the surface plate, the polishing pads are stuck in such a manner that the grooves of each polishing pad are spaced not to align with the respective grooves of the polishing pad adjacently arranged in the drive direction of the surface plate. Therefore, even though a semiconductor wafer rotates during the wafer polishing, the position of each groove in contact with the work surface of the semiconductor wafer varies every time the polishing pad in contact with the semiconductor wafer changes. This solves the first problem in which the polished surface of the semiconductor wafer has concentric portions each of which has a greater thickness than the surroundings thereof. As a result, desired surface flatness can be obtained in the wafer.

Preferably in the sticking step in the inventive method, the polishing pads are stuck in such a manner that the grooves of each said polishing pad are offset by a predetermined distance from the respective grooves of the polishing pad adjacently arranged in the drive

direction.

Preferably in the polishing step in the inventive method, the semiconductor wafer is polished with slurry containing abrasives flowing on the surfaces of the polishing pads.

A first polishing pad for a semiconductor wafer according to the present invention is intended for a polishing pad for a semiconductor wafer stuck on the surface of a belt-type surface plate. A plurality of grooves extending in the drive direction of the polishing pad are formed over the entire width from edge to edge of the polishing pad in the direction perpendicular to the drive direction.

With the first polishing pad for a semiconductor wafer, even though the polishing pad is activated by the dresser during the wafer polishing, the edge portions and the inner portion of the polishing pad are equalized in the contact area of the dresser with the polishing pad. Thus, these portions have the same pressure per unit area placed by the dresser. Even though the dresser continues to activate the polishing pad, the sectional shape of the polishing pad taken transversely of the drive direction of the pad does not become concave. This solves the second problem in which only the edge of the work surface of the semiconductor wafer is polished more deeply. As a result, desired surface flatness can be obtained in the wafer.

A second polishing pad for a semiconductor wafer according to the present invention is intended for a polishing pad for a semiconductor wafer stuck on the surface of a belt-type surface plate. In the surface of the polishing pad, a plurality of grooves extending in the drive direction of the polishing pad are formed at an angle relative to the drive direction.

With the second polishing pad for a semiconductor wafer, even though the semiconductor wafer rotates during the wafer polishing, the position of each groove in contact with the work surface of the semiconductor wafer varies according to even the travel of one polishing pad. This solves the first problem in which the polished surface of

he semiconductor wafer has concentric portions each of which has a greater thickness than the surroundings thereof. As a result, desired surface flatness can be obtained in the wafer.

Preferably in the first and second inventive polishing pads, the plurality of grooves are formed at regular intervals. This equalizes the contact times of the polishing surface of the polishing pad with all portions of the work surface of the semiconductor wafer during the wafer polishing. As a result, the polished surface of the semiconductor wafer is further planarized.

The first and second inventive polishing pads are preferably made of polyurethane foam.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1A** and **1B** show belt-polishing CMP equipment for implementing a method for polishing a semiconductor wafer according to a first embodiment of the present invention. FIG. **1A** is a perspective view schematically illustrating a polishing section of the CMP equipment, and FIG. **1B** is a plan view partly illustrating the state in which polishing pads are stuck on a surface plate.

FIG. **2A** is a sectional view illustrating a state of the polishing method of a semiconductor wafer according to the first embodiment of the present invention, in which one of the polishing pads comes into contact with the semiconductor wafer.

FIG. **2B** is a graph showing the relation between the position within the wafer and the wafer surface thickness obtained by the polishing method of a semiconductor wafer according to the first embodiment of the present invention.

FIG. **3** is a perspective view illustrating a polishing pad for use in belt-polishing CMP equipment according to a second embodiment of the present invention.

FIG. **4A** is a sectional view illustrating the state in which the polishing pad for a semiconductor wafer according to the second embodiment of the present invention comes into contact with a dresser.

FIG. **4B** is a plan view partly illustrating a plurality of the polishing pads for a semiconductor wafer according to the second embodiment of the present invention.

FIG. **5A** is a perspective view partly illustrating the state in which a polishing pad for a semiconductor wafer according to a third embodiment of the present invention is stuck on a surface plate.

FIG. **5B** is a plan view partly illustrating the state in which a plurality of the polishing pads for a semiconductor wafer according to the third embodiment of the present invention are stuck on the surface plate.

FIG. **6** is a graph showing the relation between the position within a wafer and the wafer surface thickness obtained by the polishing method of a semiconductor wafer according to the third embodiment of the present invention.

FIG. **7** is a plan view partly illustrating the state in which polishing pads for a semiconductor wafer according to a modification of the third embodiment of the present invention are stuck on a surface plate.

FIGS. **8A** and **8B** show conventional belt-polishing CMP equipment. FIG. **8A** is a perspective view schematically illustrating a polishing section of the CMP equipment, and FIG. **8B** is a perspective view illustrating a polishing pad.

FIG. **9A** is a plan view partly illustrating the state in which a plurality of the polishing pads in the conventional belt-polishing CMP equipment are stuck on a surface plate.

FIG. **9B** is a sectional view illustrating the state in which the polishing pad in the conventional belt-polishing CMP equipment comes into contact with a semiconductor wafer.

FIG. **10A** is a graph showing the relation between the position within the wafer and the wafer surface thickness obtained by using the polishing pad in the conventional belt-polishing CMP equipment.

FIG. **10B** is a plan view illustrating the polished surface of the semiconductor wafer

obtained by using the polishing pad in the conventional belt-polishing CMP equipment.

FIG. **11A** is a sectional view illustrating the state in which the polishing pad in the conventional belt-polishing CMP equipment comes into contact with a dresser. FIG. **11B** is a sectional view illustrating the state after activation process by the dresser is continuously performed.

FIG. **12A** is a sectional view of a semiconductor wafer and the polishing pad in the conventional belt-polishing CMP equipment which is obtained in the case where the activation process by the dresser is continuously performed on the polishing pad.

FIG. **12B** is a graph showing the relation between the position within the wafer and the wafer surface thickness obtained in the case where the activation process by the dresser is continuously performed on the polishing pad in the conventional belt-polishing CMP equipment.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

### (First Embodiment)

A first embodiment of the present invention will be described below with reference to the accompanying drawings.

FIG. **1A** schematically shows a structure of a polishing section of belt-polishing CMP equipment according to the first embodiment of the present invention.

As shown in FIG. **1A**, a belt-type surface plate **11** is wound around two rollers (pulleys) **10** whose rotation axes are arranged in parallel with each other. On the surface of the surface plate **11**, four sheet-shaped polishing pads **12** of which the base material is made of polyurethane are stuck. Polyurethane used for the base material of the polishing pads **12** is preferably closed-cell polyurethane foam.

A method for polishing a semiconductor wafer **20** adhering by suction to a carrier **13** is as follows. With the surface plate **11** driven in a predetermined direction, slurry **15** containing abrasives is supplied from a nozzle **14** onto the surface (polishing surface) of

the polishing pad **12**. With the surface of the semiconductor wafer **20** rotated, the surface (the work surface) of the semiconductor wafer **20** is pressed against the surface of the polishing pad **12**. In order to activate the surfaces of the polishing pads **12**, a dresser **17** equipped on the bottom of a cylinder **16** is moved, whenever necessary, in the direction perpendicular to the drive direction of the surface plate **11** with the dresser **17** pressed against the polishing pad **12**.

As shown in the enlarged plan view in FIG. **1B**, each of the polishing pads **12** according to the first embodiment has grooves **12a** extending in the same direction as the drive direction of the surface plate **11**. The polishing pads **12** adjacently arranged in the drive direction of the surface plate **11** are stuck apart in such a manner that the grooves **12a** of one polishing pad **12** are spaced not to align with the respective grooves **12a** of the other polishing pad **12**. Note that the grooves **12a** serve to efficiently supply the slurry **15** onto the surface of the semiconductor wafer **20**.

As described above, the polishing pads **12** adjacently arranged in the drive direction of the surface plate **11** are stuck in such a manner that the grooves **12a** of one polishing pad **12** are spaced not to align with the respective grooves **12a** of the other polishing pad **12**. In accordance with the foregoing, in FIG. **2A**, the grooves **12a** provided in one polishing pad **12** (shown with solid lines) are offset from the grooves **12a** provided in another polishing pad **12** (shown with broken lines) next to one said polishing pad **12**, so that all the portions of the work surface of the semiconductor wafer **20** come into contact reliably with any one of the polishing surfaces of the polishing pads **12** even though the semiconductor wafer **20** is rotating. Thus, even when the center portion of the semiconductor wafer **20** in FIG. **2A** is not polished by the grooves **12a** of one said polishing pad **12** immediately after the initiation of polishing, the center portion is surely polished by the grooves **12a** of another said polishing pad **12**. Consequently, this eliminates the unpolished portion of the work surface of the semiconductor wafer **20** which is located at the center thereof.

Note that there is no limit to the number of polishing pads **12** stuck on the belt-type

surface plate **11**. However, in the first embodiment, the four polishing pads **12** are stuck in such a manner that the grooves **12a** of each polishing pad **12** are offset from the respective grooves **12a** of the adjacent polishing pad **12** in a pitch with a half width of each groove **12a**. This equalizes the time the grooves **12a** of the polishing pads **12** do not polish the semiconductor wafer **20** as well, so that no unpolished portion exists in the center portion of the semiconductor wafer **20**. As a result, the entire work surface of the semiconductor wafer **20** can be polished uniformly.

(Second Embodiment)

A second embodiment of the present invention will be described below with reference to the accompanying drawings.

FIG. **3** shows a polishing pad used in belt-polishing CMP equipment according to the second embodiment of the present invention.

As shown in FIG. **3**, a polishing pad **12** according to the second embodiment has a plurality of grooves **12a** formed on the polishing surface thereof. The grooves **12a** extend in parallel with one other in the drive direction of the polishing pad **12**, and they are provided over the entire width from edge to edge of the polishing surface in the direction perpendicular to the drive direction of the polishing pad **12**.

When the polishing pad **12** of this formation polishes a semiconductor wafer, the inside portion **A** and the edge portion **B** of the polishing pad **12** are equalized in the contact area of the polishing surface thereof with a dresser **17** as shown in the sectional view in FIG. **4A**. Therefore, the dresser **17** can activate the entire polishing surface of the polishing pad **12** uniformly. This prevents a large removal of only the inside portion **A** of the polishing pad **12** in the activation by the dresser **17**. Consequently, as shown in FIG. **2B**, the polishing pad can polish the peripheral portion of the semiconductor wafer no thinner than the center portion thereof, and therefore the polishing pad can polish the entire work surface of the semiconductor wafer uniformly.

As shown in FIG. **4B**, the polishing pads **12** adjacently arranged in the drive direction thereof are stuck in such a manner that the grooves **12a** of one polishing pad **12** are spaced not to align with the respective grooves **12a** of the other polishing pad **12**, which prevents the center portion of the polished semiconductor wafer from being thickened as compared to the surroundings thereof.

(Third Embodiment)

A third embodiment of the present invention will be described below with reference to the accompanying drawings.

FIG. **5A** shows a polishing pad used in belt-polishing CMP equipment according to the third embodiment of the present invention.

As shown in FIG. **5A**, a polishing pad **12** according to the third embodiment has a plurality of grooves **12b** extending in parallel with one other in the drive direction of the polishing pad **12**. The grooves **12a** are inclined at a predetermined angle θ relative to the drive direction of the polishing pad **12**. The predetermined angle θ is set to such an extent that the essential functionality of the grooves in which the grooves ensure an efficient supply of slurry delivered from a nozzle onto the polishing pad **12** does not deteriorate, preferably at about 1 to 15°. The grooves **12b** provided in the polishing pad **12** are formed over the entire width from edge to edge of the polishing surface in the direction perpendicular to the drive direction of the polishing pad **12**. In the case where a plurality of the polishing pads **12** are stuck on the surface of a surface plate **11**, a gap must be provided between the polishing pads **12** adjacently arranged in the drive direction thereof.

Using the polishing pad **12** according to the third embodiment, a semiconductor wafer is polished. Then, as can be seen from the graph in FIG. **6** illustrating the relation between the position within the wafer and the wafer surface thickness, there is no unpolished portion in the center of the semiconductor wafer and in addition there is no thinned peripheral portion in the semiconductor wafer. Therefore, a uniform surface

thickness can be attained in the entire polished surface of the semiconductor wafer.

(Modification of Third Embodiment)

As shown in FIG. 7, in the case where a plurality of polishing pads **12** are stuck on the surface of a surface plate **11**, grooves **12b** provided in the respective polishing pads **12** are disposed in a zigzag arrangement in which the grooves **12b** of each polishing pad **12** are inclined in an opposed direction to the direction of inclination of the grooves **12b** provided in the adjacent polishing pad **12** relative to the drive direction of the polishing pads **12**. This further improves the flatness of the polished surface of a semiconductor wafer.